Professional H.265/HEVC Encoder LSI Toward High-Quality 4K/8K Broadcast Infrastructure

Innovative R&D by NTT

Code Name: NARA (Next-generation encoder Architecture for Real-time HEVC Application)

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Outline

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  - Requirements for 4K/8K broadcasting
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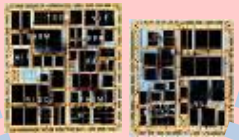
History of NTT's video CODEC LSIs

Analog *Digital* → SDTV *HDTV* → MPEG2 *H.264* → HDTV *UHDTV* / H.264 *H.265*

Encoder PCI Board

Portable HDTV Encoder (ICCE2001)

Encoder PC Card (ICCE2000)



ENC-C/-M ('95) (HotChips7)

SuperENC ('98) (HotChips10)

SuperENCII('00)

VASA ('02) (HotChips14)

NHK/NTT-COM Board

HDTV MPEG-2 Encoder

HDTV MPEG-2 Decoder

ISIL-II ('07) (CoolChips X)

ISIL('02) (CICC2003)

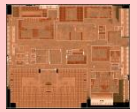
MPEG-2/H.264 Transcoder

HDTV H.264 Encoder

HDTV H.264 Decoder

SARA('07) (HotChips19)

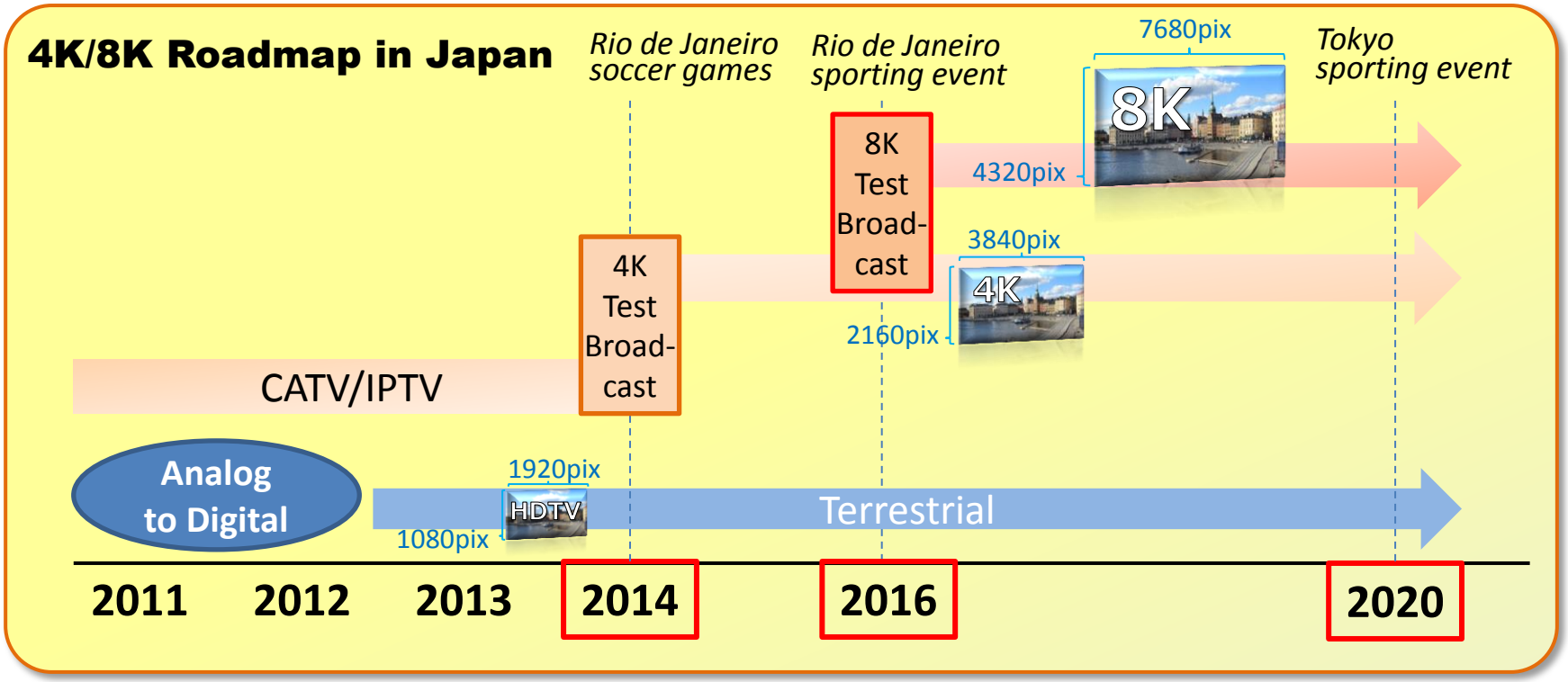
SARA/D ('08) (CoolChips XI)



NARA('15)

Roadmap toward 4K/8K UHDTV

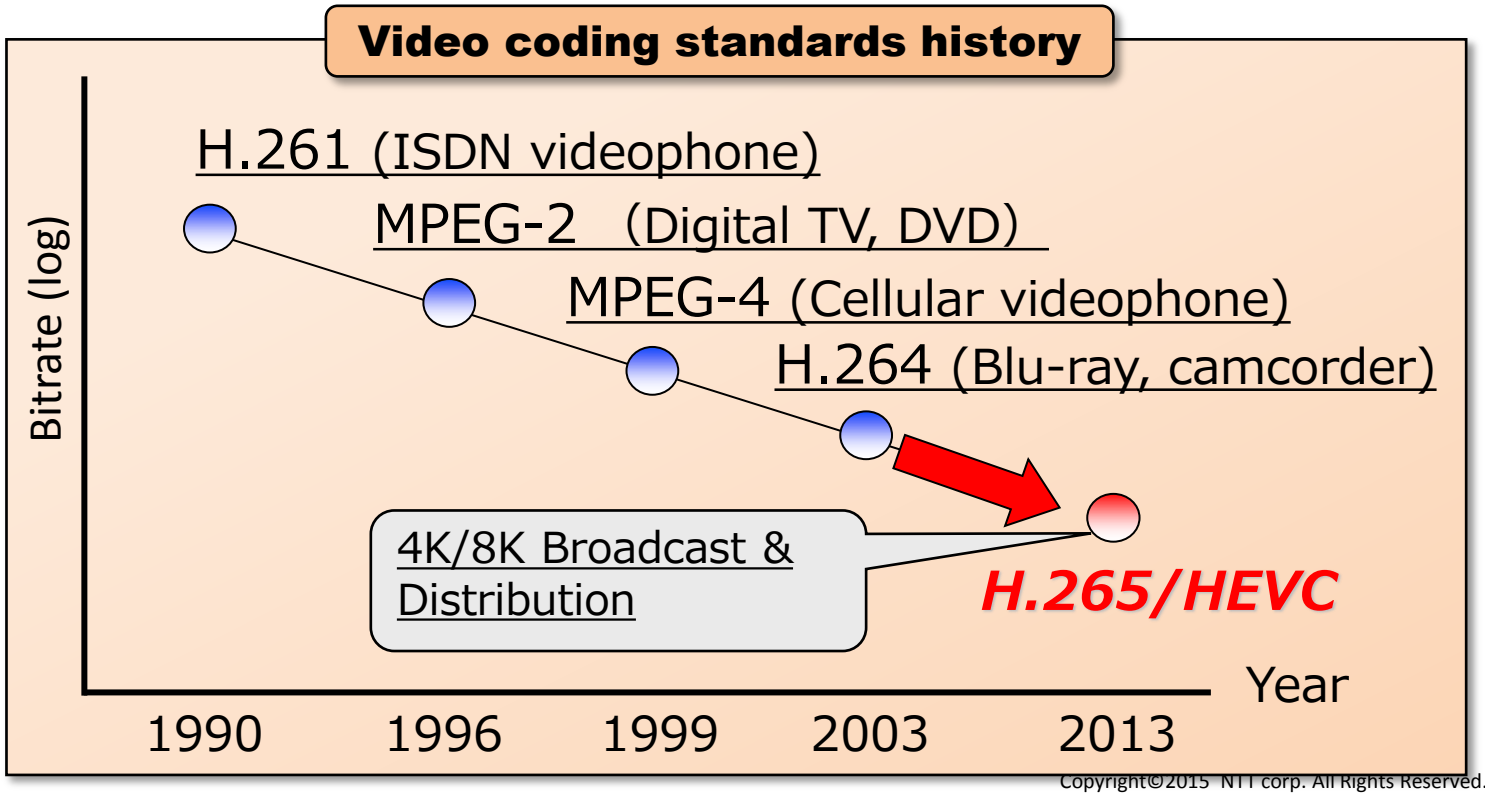
- 4K test broadcast over satellite in 2014, 8K in 2016
- 4K/8K commercial broadcast TV programs in 2020



Reference: Interim Report of 4K/8K Roadmap Follow-up Meeting (MIC, Japan)

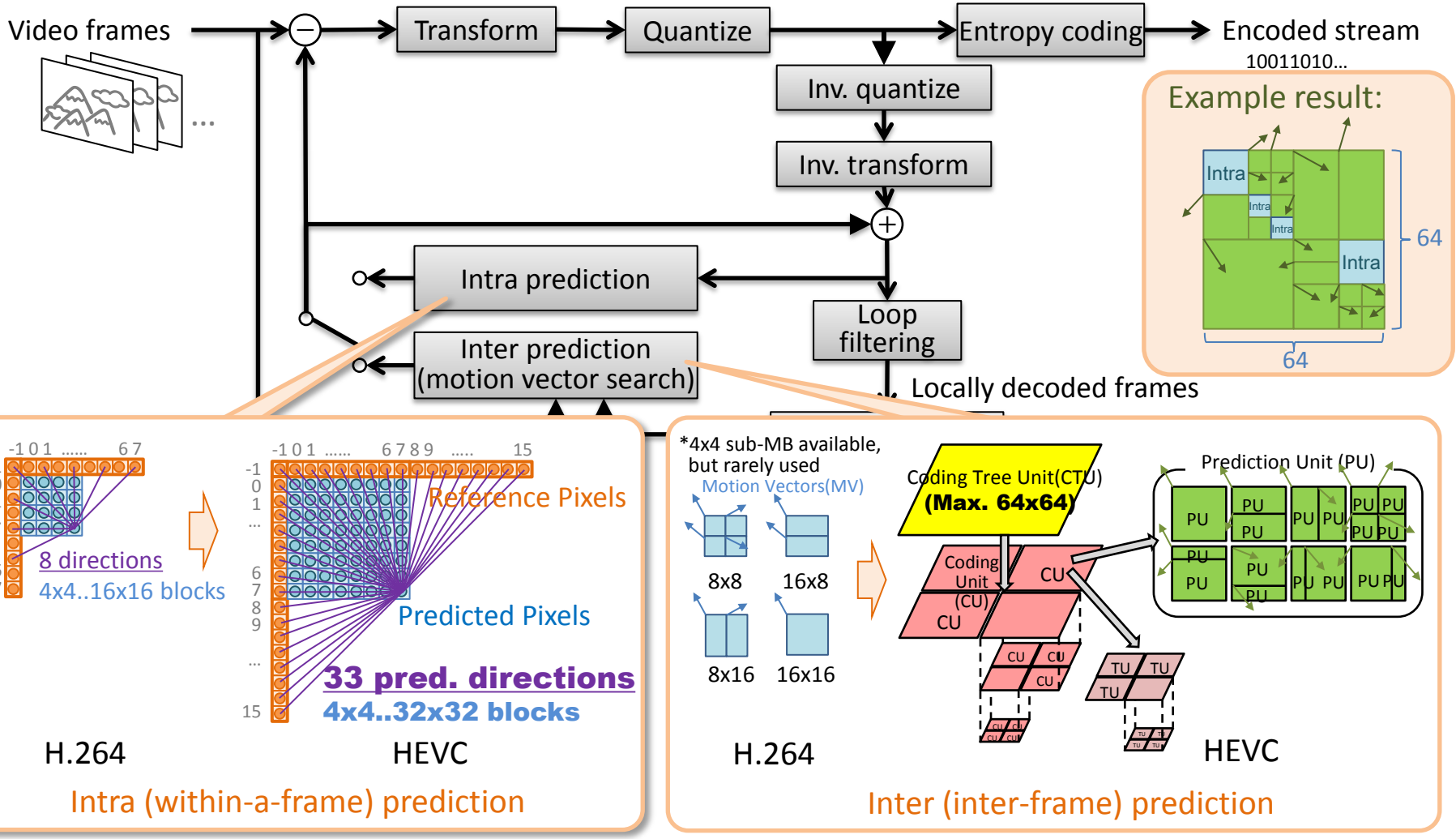
HEVC – High Efficiency Video Coding

- The latest video coding standard (Jan. 2013, Range extensions Apr. 2014)
- Achieves half bit rate compared to H.264, 1/4 to MPEG-2, key technology for 4K/8K



What is HEVC?

- Existing encoding flows, but “adaptive and exhaustive” combination of prediction tools



HEVC encoding complexity

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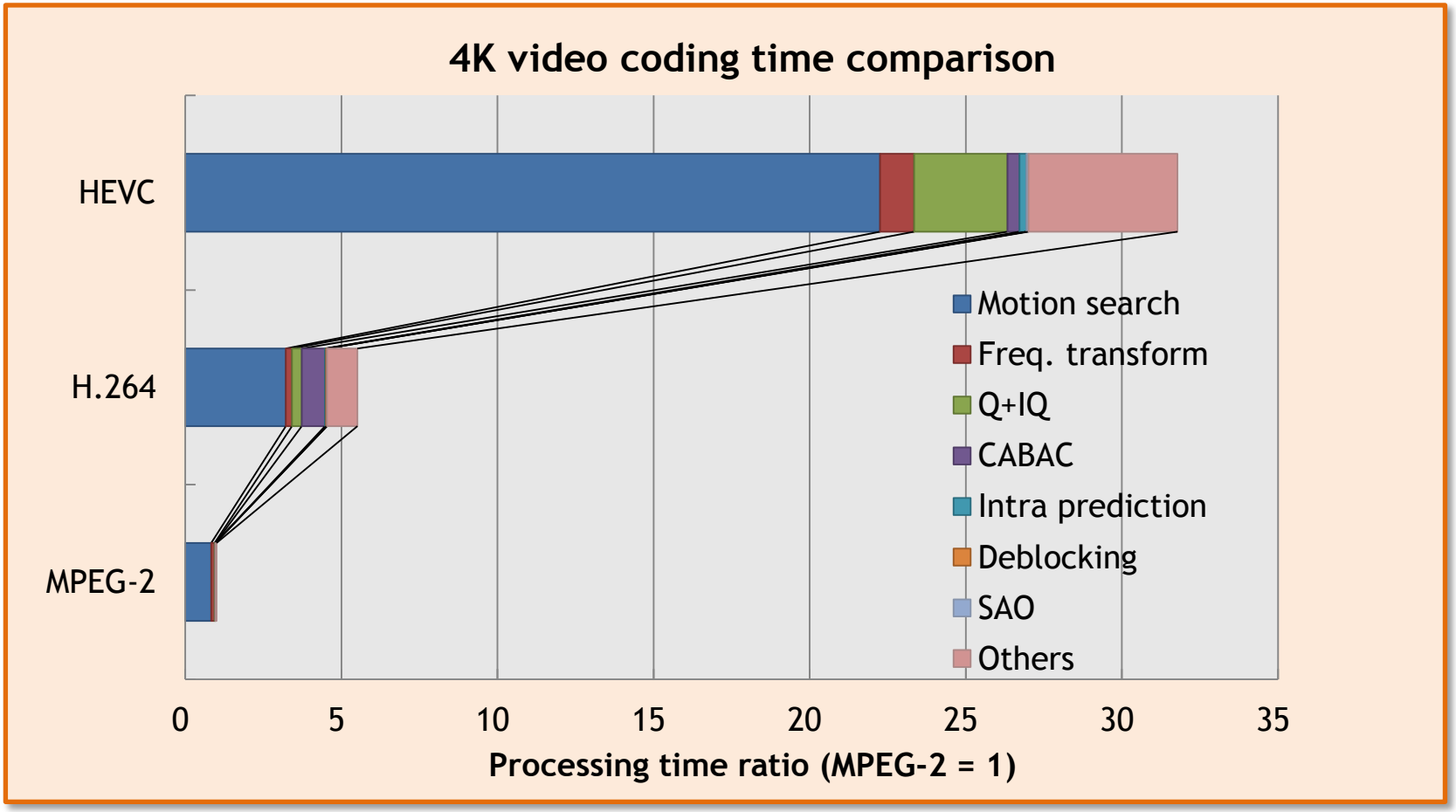
- About 30x of MPEG-2 processing time, 5x of H.264 processing time



Reference software: MPEG-2_MSSG H.264_JM18.5 HEVC_HM12.1

Requirements for 4K/8K broadcasting

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- Practical 4K/8K broadcast infrastructure in 2020
- Latest video coding standard (H.265/HEVC) for high compression
- Color signal robustness against tandem encoding
- High bitrate of up to 600 Mbps

NARA: Professional H.265/HEVC encoder LSI toward high-quality 4K/8K broadcast infrastructure

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Main concepts for NARA architecture

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- Application specific hardware blocks for processes high computational complexity processes, such as precise motion estimation
- Hierarchical pipeline scheme for decisions on optimal hierarchical coding/prediction/transform unit size with high compression
- Single-chip 4K configuration and multi-chip 8K configuration for practical encoding systems

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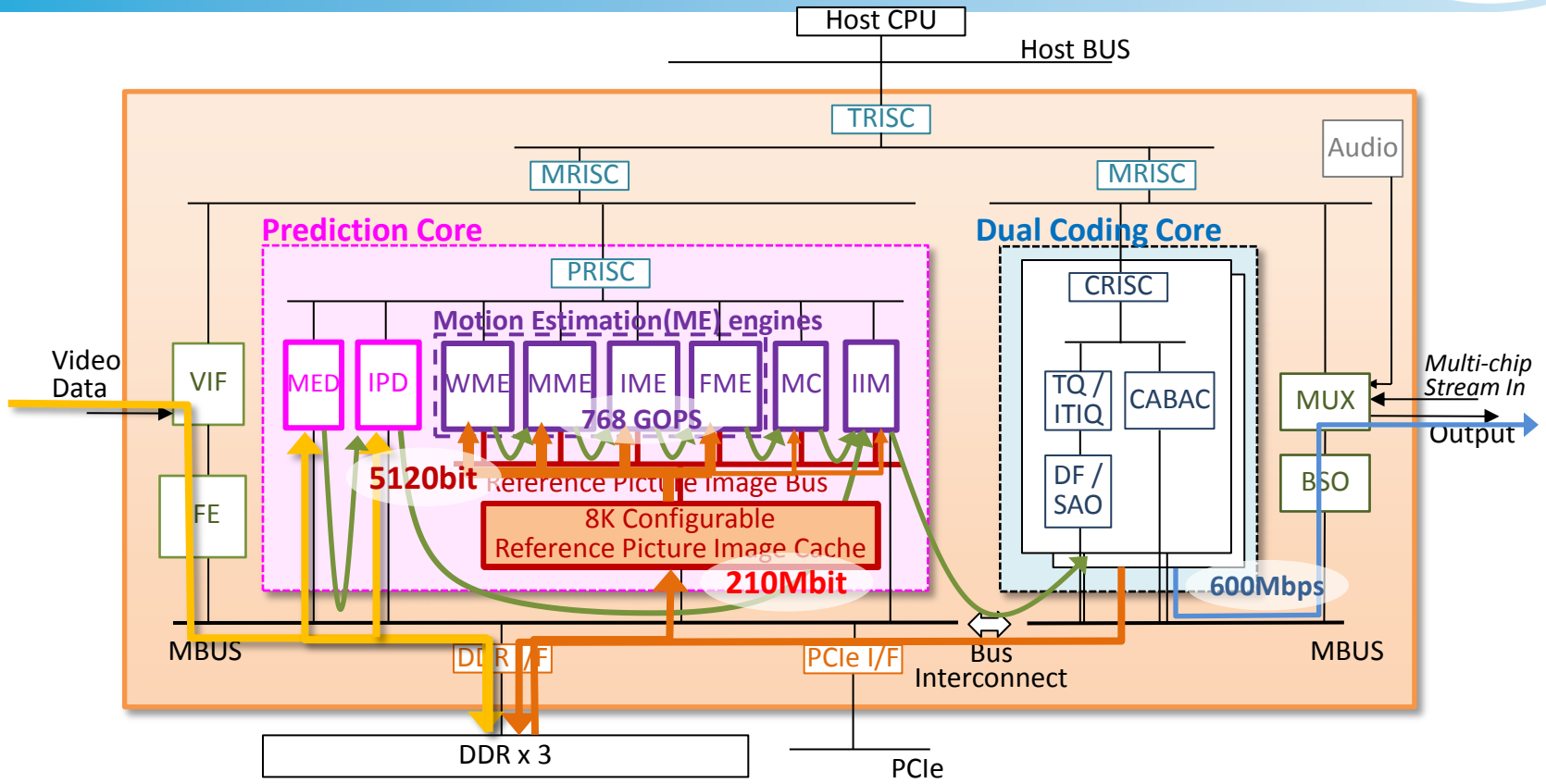
NARA block diagram



VIF: Video Interface
IFE: Image Feature Extraction
MED: Multi-block-size Edge Detector
IPD: Intra Prediction
WME: Wide-range Motion Estimation
MME: Multi-Block-Size Motion Estimation
IME: Integer pixel Motion Estimation
FME: Fractional pixel Motion Estimation

MC: Motion Compensation
IIM: Intra-Inter Mode Decision
MBUS: Memory BUS
TQ: Transform and Quantization
ITIQ: Inverse Transform and Quantization
DF: Deblocking Filter
SAO: Sample Adaptive Offset filtering

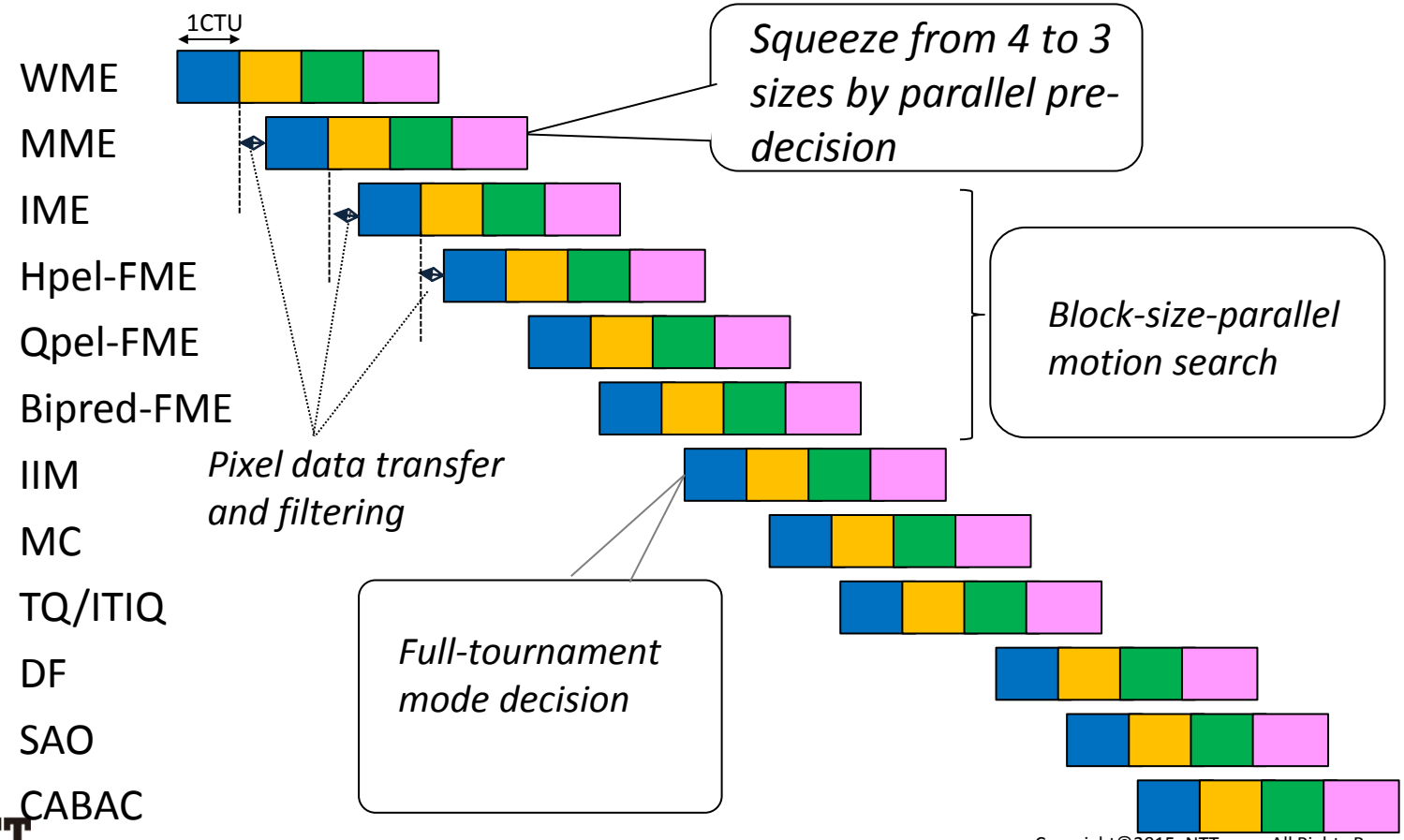
BSO: Bit Stream Out
MUX: Multiplexer
PRISC: Prediction Core RISC
CRISC: Coding Core RISC
MRISC: Middle-level RISC
TRISC: Top-level RISC

NARA pipeline polices

- Parallel processing for precise motion estimation achieving better coding efficiency
- Strictly sequential calculation (conforming to HEVC standard) desirable for mode decision to precisely evaluate coding bit costs
- Short pipeline stages for efficient rate control

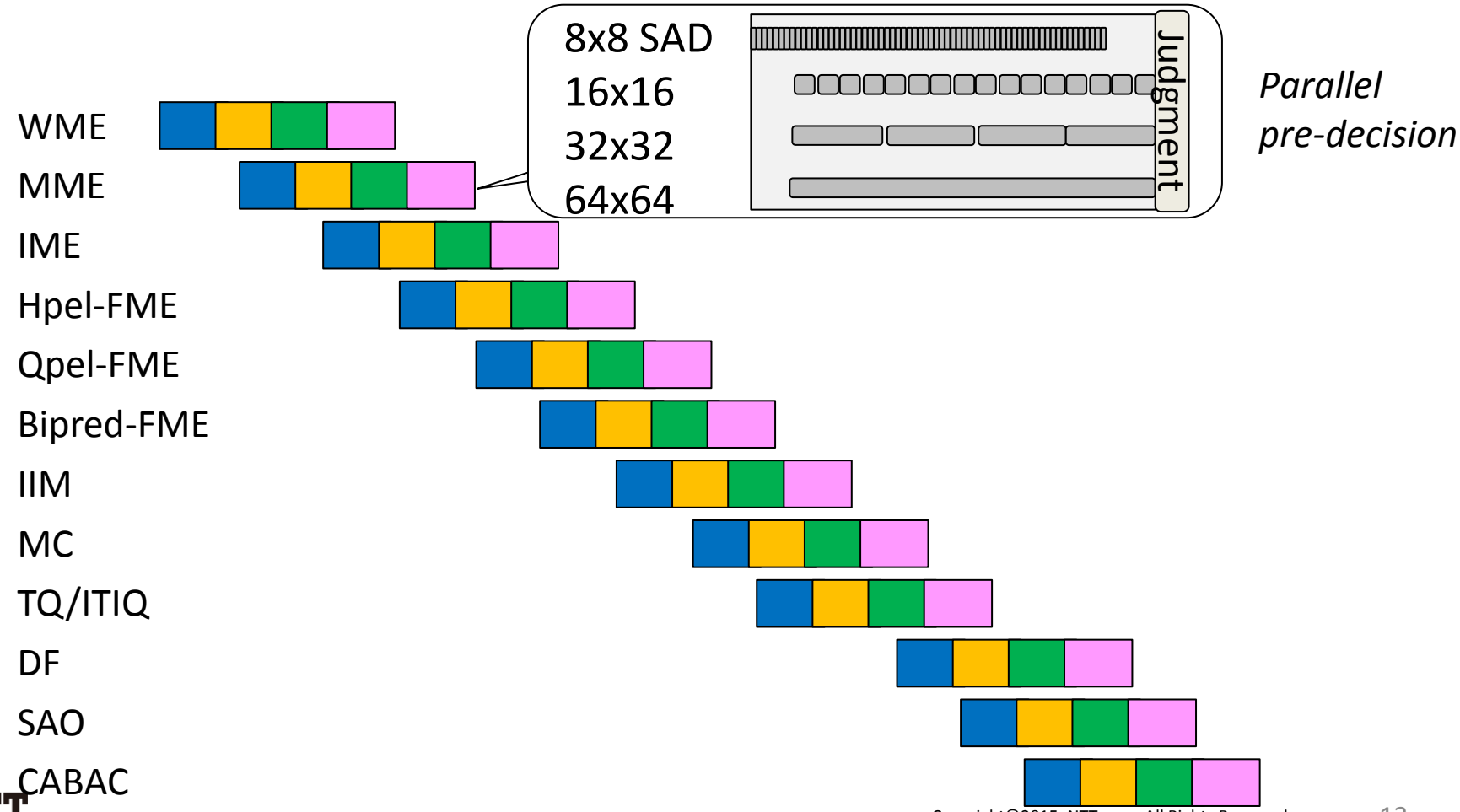
NARA pipeline scheme

- NARA adopts CTU-based hierarchical pipeline scheme
- Filter mode decisions for coding efficiency while keeping image quality:
  - Wide-range ME (WME) -> Multi-block-size ME (MME) -> Integer ME (IME) -> Fractional ME (FME) -> Inter/Intra Mode Decision (IIM)



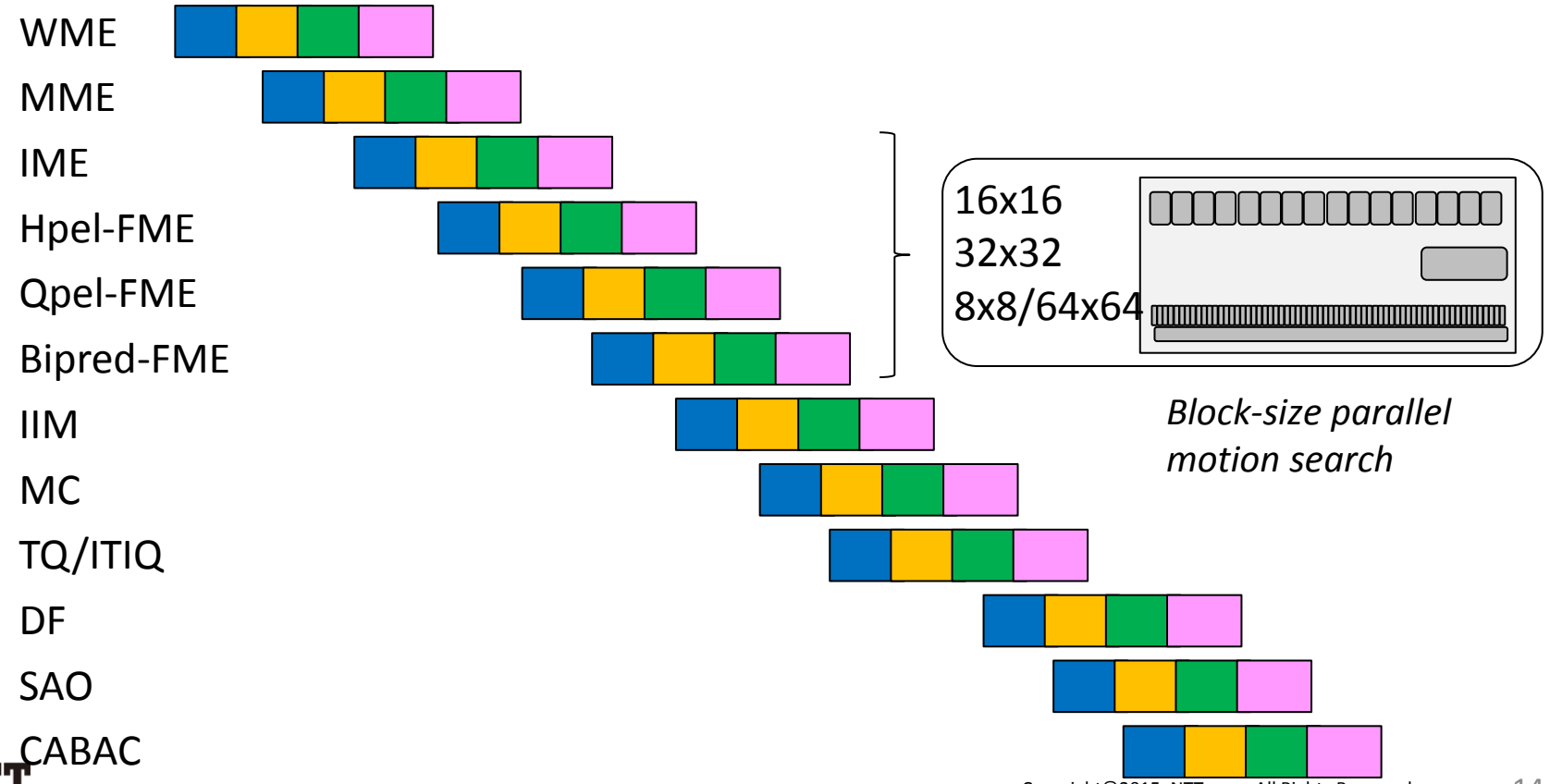
Parallel pre-decision in MME

- Motion estimation for all block sizes by parallel pre-decision
- Filter into three block sizes by parallel pre-decision



Block-size parallel motion search in FME

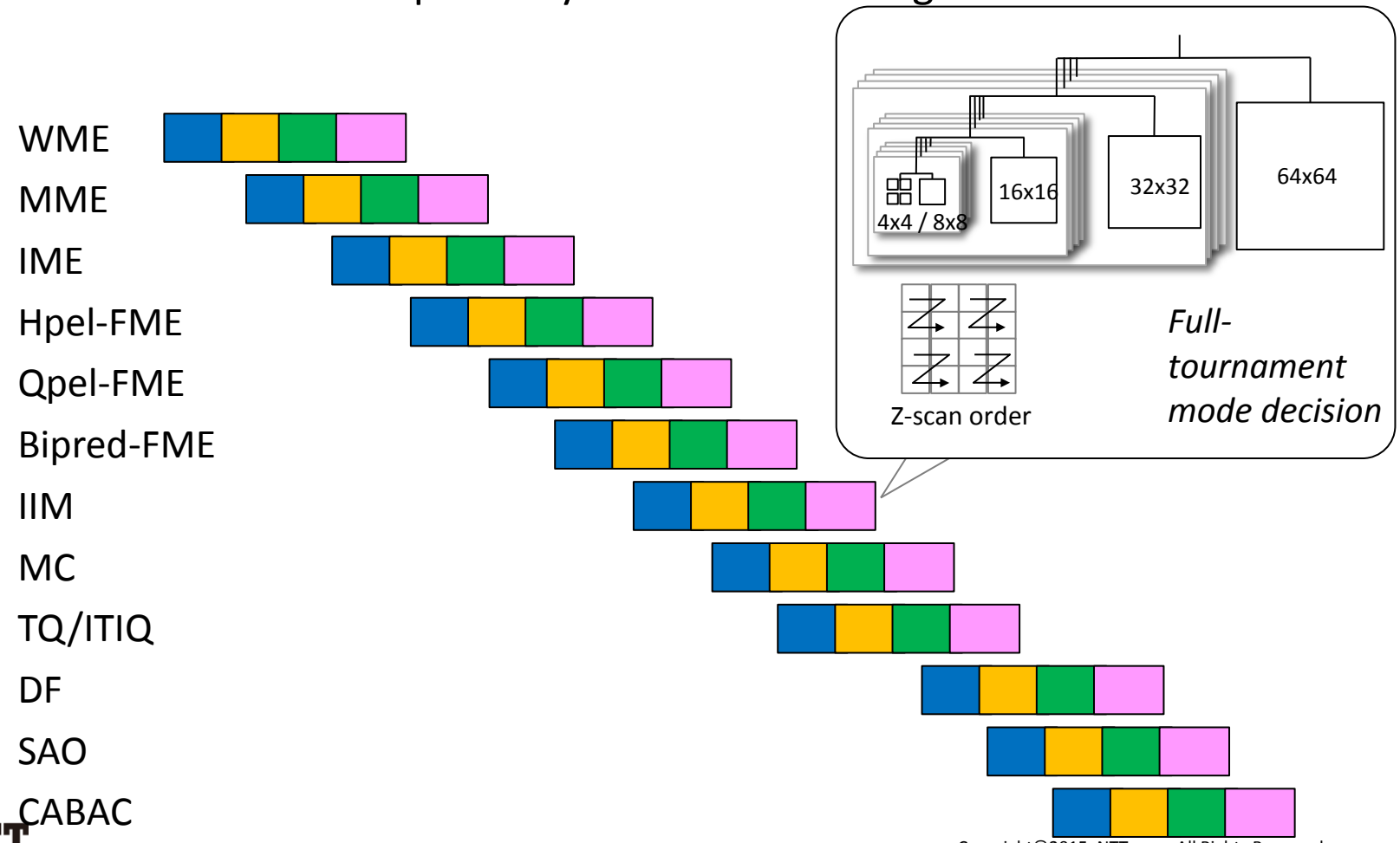
- Motion estimation for 3 block sizes in block-size parallel motion search



Block-size parallel motion search

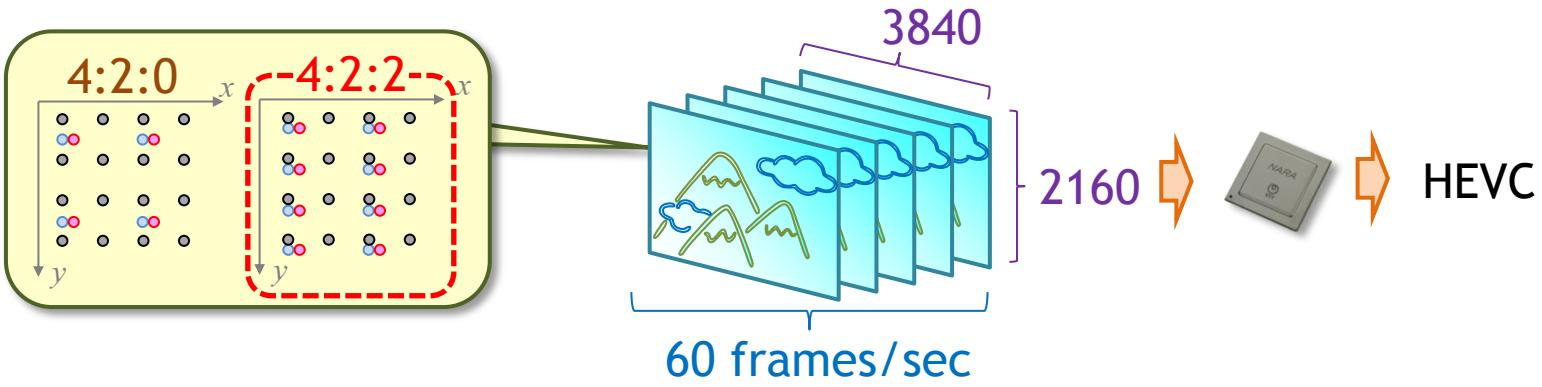
Full-tournament mode decision in IIM

- Strictly sequential calculation by full-tournament mode decision
- Strictly sequential calculation (conforming to HEVC standard) desirable for mode decision to precisely evaluate of coding bit costs

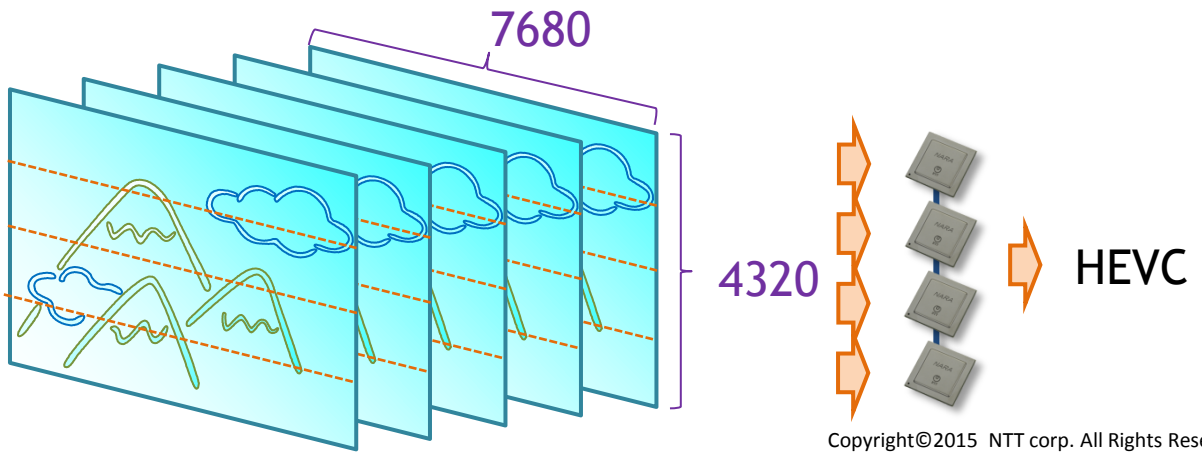


NARA configurations

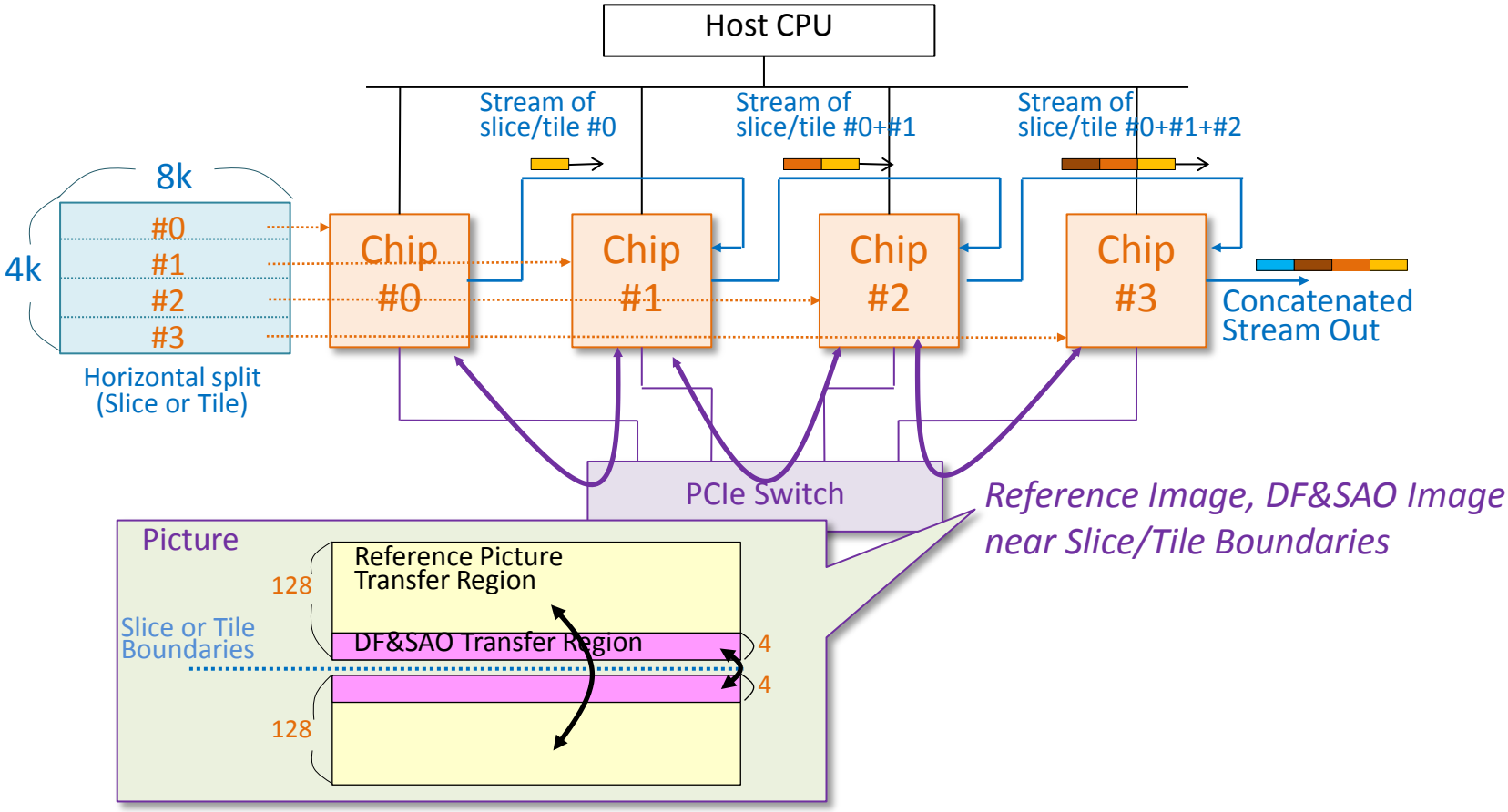
- Capability
  - Single-chip processing up to 4K 60fps 4:2:2



  - Multi-chip scalability up to 8K 60fps



Multi-chip configuration



Key NARA features and functions

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Single-chip configuration:

- Complicated HEVC processing mapped to hierarchical pipeline scheme based on coding tree units (CTUs).
- Hierarchical pipeline achieves wide-range motion estimation with ±3847.75 x ±1926.75 search range and optimized HEVC's high-precision prediction mode decision
- 4k/60p 4:2:2 real-time encoding with ultra-low delay for field pickup units (FPUs), high bitrate of up to 600 Mbps for contribution, multi-channel encoding for cloud systems, and multi-standard encoding for smooth migration

Multi-chip configuration:

- Ultra-high definition TV encoded beyond 4K with motion estimation and loop filtering across split boundaries when each chip encodes a partitioned frame
- Suitable for HEVC-based tandem encoding with 4:2:2 for keeping good color information and two-pass encoding for higher compression of final distribution

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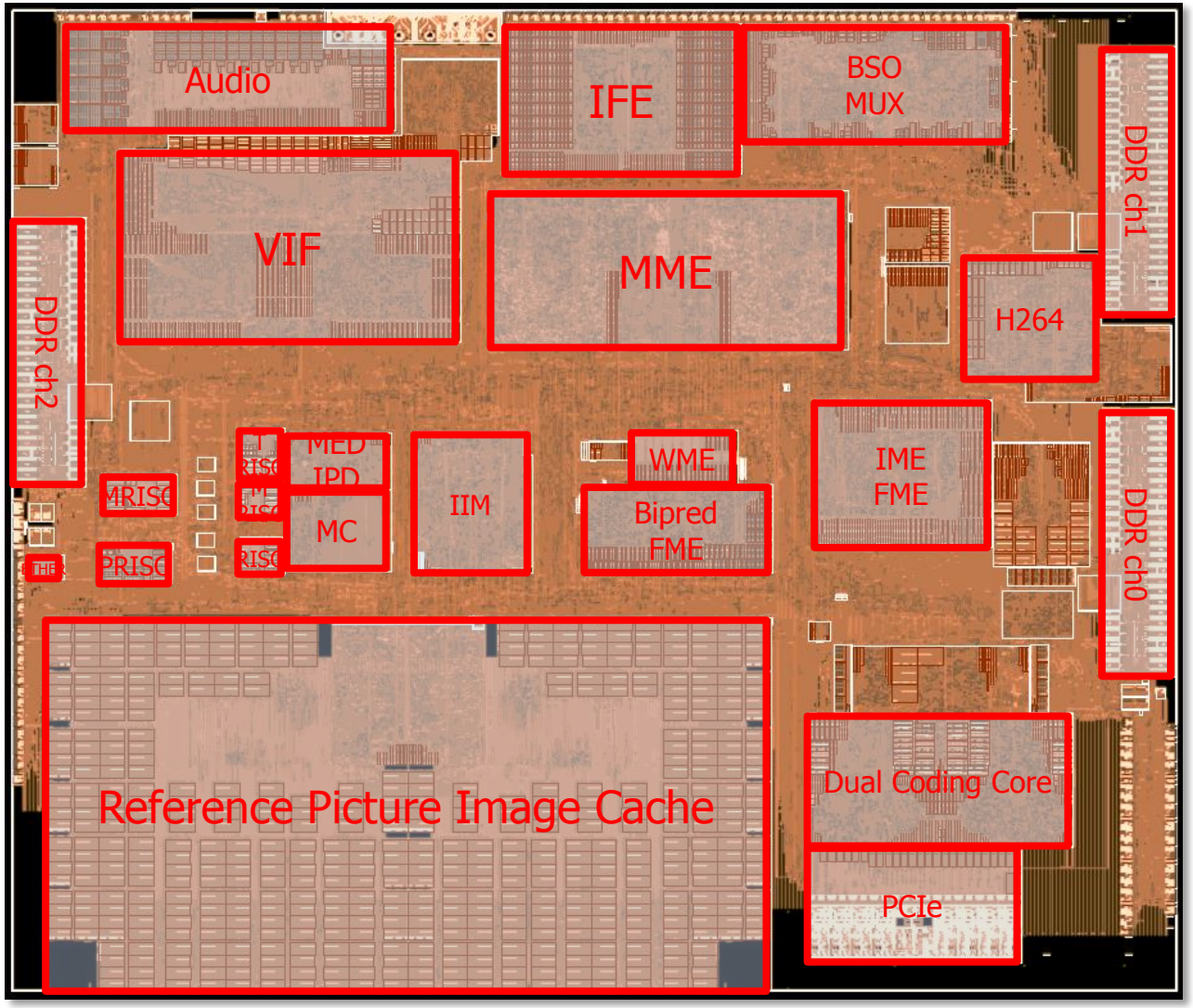
NARA chip implementation



Physical features

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Technology	28nm CMOS
Number of transistors	83M gates
Clock frequency	Max 600 MHz
Supply voltage	Core: 0.9 V IO: 1.8/3.3 V DDR3: 1.5 V PCIe and 3G-SDI: 0.9/1.8 V
Power consumption	Approximately 15.0W
Package	1152 pin FCBGA (35 x 35mm)
External memories	DDR3

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Functional features

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Video	Profile	H.265/HEVC Main, Main 10, Main 4:2:2 10 H.264/AVC Baseline, Main, High, High422
	Motion search range	-3847.75/+3847.75 (H) -1926.75/+1926.75 (V)
	Resolution and video rate	Single-chip: 4096x2160 at up to 60 frames per second Multi-chip: 7860x4320 at up to 60 frames per second
Others	Audio: Serial I/F x 2 Port Stream Out: Parallel x 1 /Serial x 4 PCIe: Gen.2 x 8 Lane Ethernet: 1000/100/10 Mbps with MAC Others: User PES input, STC input/output	

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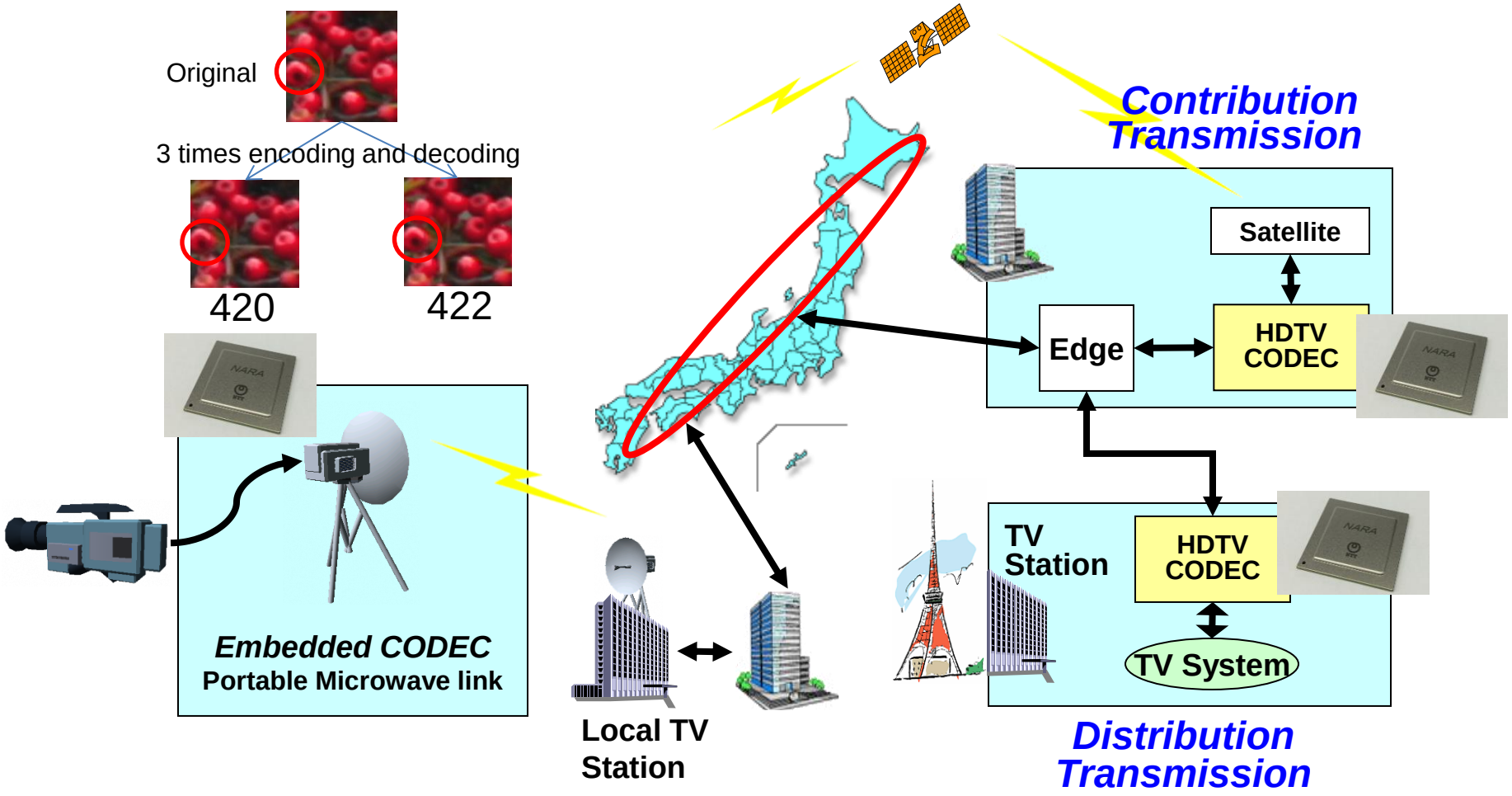
Target applications (1)

Digital TV Broadcasting Network Service



Target applications (2)

- Museums, galleries

- Digital cinema (Projectors, screens)
- Box office sales

- Conferencing systems/services
- Projectors

- Security (surveillance) cameras
- Industrial camera sensors

- CAD, CAM, CG (Mechanical, automotive, industrial designs)

- Medical monitors
- Endoscopic systems

- Digital signage
- Outdoor display LEDs

- Mobile phones
- Consumer TVs
- Broadcast devices (Cameras, editors, encoders)

Reference: Interim Report of 4K/8K Roadmap Follow-up Meeting (MIC, Japan) *1USD= 120JPY

Conclusion

- Developed: single-chip 4K 60fps 4:2:2 HEVC video encoder LSI, scalable to 8K 60fps
- 8K scalability achieved inter-chip connectivity and parallel processing functions
- NARA architecture has hierarchical pipeline scheme for CTUs

NARA is a key LSI for professional H.265/HEVC encoder LSI toward high-quality 4K/8K broadcast infrastructure